the top (adjacent silicon nitride and oxide layer **16** and **15**, respectively) by bridging provided by shallow trenches. Accordingly, shallow trenches are etched through layers **21**, **16** and **15** and into N^- layer **14** at locations **22** and **23** as shown in FIG. **4**.

Additionally, shallow trenches are etched into the tops of the polycrystalline silicon filling within deep trenches **18**, **19** and **20** so that better coplanarity is achieved in the next following oxidation step.

After the shallow trenches are etched, the resulting structure is thermally oxidized to convert the exposed polycrystalline silicon in deep trenches **18**, **19** and **20** and to convert the exposed monocrystalline silicon (N^- layer) in shallow trenches **22** and **23** to silicon dioxide. The thermal oxidation converts at least the top portion of the polycrystalline silicon in deep trenches **18**, **19** and **20** into thermal oxide approximately as thick as the thermal oxide formed in shallow trenches **22** and **23** thereby eliminating any "weak spots" that might have formed near the center of the polycrystalline silicon filled deep trenches **18**, **19** and **20** at the conclusion of the polycrystalline silicon deposition step. It is not necessary that the thermal oxidation be continued to completely convert all of the polycrystalline silicon within deep trenches **18**, **19** and **20** into silicon dioxide. Any residual polycrystalline silicon that might remain after oxidation, such as within regions **24**, **25** and **26**, are completely surrounded by a protective combination of CVD oxide **21** and thermally grown silicon dioxide.

Having thus described my invention, what I claim as new, and desired to secure by Letters Patent is:

1. The method for forming narrow, deep, recessed oxide isolation filled trenches and wide, deep recessed oxide isolation filled trenches in a monocrystalline silicon substrate comprising:

etching said substrate through mask apertures in a masking layer defining said narrow trenches and the perimeters of said wide trenches,

thermally oxidizing the surfaces of said trenches,

partially filling said trenches with a dielectric material,

completing the filling of said trenches with polycrystalline silicon,

etching said substrate through mask apertures in the masking layer defining shallow trenches, some of said shallow trenches coinciding with the upper regions of said filled deep trenches and others of said shallow trenches bridging between said filled deep trenches, and thermally oxidizing the remaining polycrystalline silicon in said deep trenches and the monocrystalline silicone in said shallow trenches.

2. The method defined in claim **1** and further including removing said polycrystalline silicon covering substrate areas other than said deep trench areas prior to etching said substrate through mask apertures defining said shallow trenches.

3. The method defined in claim **1** wherein said dielectric material comprises chemical vapor deposited silicon dioxide.

4. The method defined in claim **1** wherein said masking layer comprises a layer of silicon dioxide covered by a layer silicon nitride.

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